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=> s 395/?/ccls or 370/?/ccls
           35978 395/?/CCLS
          16433 370/?/CCLS
L1        51429 395/?/CCLS OR 370/?/CCLS

=> s l1 and network?/ab
          21491 NETWORK?/AB
L2         6191 L1 AND NETWORK?/AB

=> s l2 and fifi?/ab
              0 FIFI?/AB
L3            0 L2 AND FIFI?/AB

=> s l2 and fifo?/ab
            634 FIFO?/AB
L4           49 L2 AND FIFO?/AB

=> s l2 and (pipeline? (2a) buffer?)/ab
           4381 PIPELINE?/AB
          13477 BUFFER?/AB
             18 (PIPELINE? (2A) BUFFER?)/AB
L5            1 L2 AND (PIPELINE? (2A) BUFFER?)/AB

=> s l4 and (full? or empty?)/ab
          36086 FULL?/AB
           5821 EMPTY?/AB
L6            8 L4 AND (FULL? OR EMPTY?)/AB

=> d l5 kwic

US PAT NO:     5,175,732 [IMAGE AVAILABLE]          L5: 1 of 1
US-CL-CURRENT: 370/463
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ABSTRACT:
Method and apparatus are provided for data communication control within the communication controllers of stations within a local area **network**. In general, the method and apparatus involves maintaining within the command and status control interface unit of the communication controller,. . . well as transmitted. Each receive command is uniquely associated with a data packet storage location. Receive and transmit commands are **buffered** in a **pipeline** manner in the rece
ive and transmit command queues, respectively,
whereas receive and transmit status bits are **buffered** in a **pipeline** manner in the receive and transmit status queues, respectively. The processor interfacing with the communication controller buffers transmit and receive. . . these commands. The media access control unit of the communication controller executes each command when it is ready according to **network** protocol, and generates status bits which are buffered in respective status bit queues. The status bits are selectively processed to. . . processor. Consequently, the minimum back-to-back separation between two communication events of the same type, is eliminated thereby improving node and **network** data throughout.

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=> d l6 kwic 1-8
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US PAT NO: 5,568,470 [IMAGE AVAILABLE] L6: 1 of 8
US-CL-CURRENT: **370/238**, **395**, **412**

ABSTRACT:
In . . . ATM cells can experience a small delay from the ATM layer to the PHY layer to transmission on the ATM **network**. Such an arrangement includes providing the endnode with an ATM layer, the ATM layer having a first-in-first-out (**FIFO**) queue for transmitting transmit ATM traffic, providing the endnode with a PHY layer, the PHY layer having a **FIFO** queue for receiving the transmit ATM traffic, providing an interface between the **FIFO** queue of the ATM layer and the **FIFO** queue of the PHY layer for the flow of the transmit ATM traffic, providing a signal in the ATM endnode,. . . the state machine monitoring the signal in the ATM endnode, stalling the transfer of the transmit ATM traffic from the **FIFO** of the ATM layer to the **FIFO** of the PHY layer over the inter
face when the signal and the state
machine indicate that the **FIFO** of the PHY layer is **full**, and transmitting the transmit ATM traffic from the **FIFO** of the ATM layer to the **FIFO** of the PHY over the interface. By causing the ATM layer to generate/transfer a continuous stream of cells to the PHY layer, the method can provide cell time indications to allow the ATM layer to synchronize itself to the **network**.

US PAT NO: 5,566,175 [IMAGE AVAILABLE] L6: 2 of 8
US-CL-CURRENT: **370/468**; **395/250**

ABSTRACT:
This invention relates to the efficient use of resources in broadband telecommunications **networks** when handling bursty data traffic. A new technique shapes the data traffic profile to efficiently maximize the bandwidth reservation scheme whilst minimizing data loss and delay. The Fast Bandwidth Reservation Shaper (FBRS) comprises a **FIFO** buffer with three thresholds (T1-T3), a server, and a Fast Reservation Protocol (FRP) control function which monitors the state of. . . the queue and its associated thresholds, alters the service rate of the server, and handles the FRP protocol. With an **empty** buffer, a zero or small bandwidth is allocated to the data connection. When the first buffer threshold is reached, the FRP controller attempts to negotiate a small data rate (R1) with the **network**. As the queue grows to the second threshold (T2), the FRP controller attempts to negotiate a higher data rate (R2),. . .

US PAT NO: 5,563,885 [IMAGE AVAILABLE] L6: 3 of 8
US-CL-CURRENT: **370/391**, **394**, **395**, **411**, **413**, **538**

ABSTRACT:
A method and system for scheduling multiple channel data output. A multi-channel data processor stores ATM cells received from a **network** data input stream in channel **FIFOs** of a cell buffer. The input interval between cells received at a channel **FIFO** and the channel **FIFO fullness** is monitored to determine an optimum cell output interval for each channel. This optimum cell output interval is established such. . . the rate at which cells are output is substantially constant compared to the input cell rate and drives each channel **FIFO fullness** towards a nominal value. Optimum cell departure times are then calculated based on the optimum cell output interval for each. . . cell departure times are sorted and prioritized to create an overall optimum cell transmission schedule. By removing cells from channel **FIFOs** according to this optimal cell transmission schedule, data returns to the **network** having a restored temporal sequence in each channel without requiring embedded timing information. Establishing an output rate and sequence which optimizes **FIFO fullness** and minimizes gaps in the output data, also reduces buffering requirements for downstream **network**

equipment.

US PAT NO: 5,485,584 [IMAGE AVAILABLE] L6: 4 of 8
US-CL-CURRENT: **395/842**; 364/244.3, 247, 247.3, 247.7, DIG.1; **395/200.01**, **500**

ABSTRACT:
In a Local Area **Network** (LAN) system, an ethernet adapter exchanges data with a host through programmed I/O (PIO) and **FIFO** buffers. The receive PIO employs a DMA ring buffer backup so incoming packets can be copied directly into host memory when the PIO **FIFO** buffer is **full**. The adapter may be programmed to generate early receive interrupts when only a portion of a packet has been received from the **network**, so as to decrease latency. The adapter may also be programmed to generate a second early interrupt so that the. . . to the adapter, which further reduces latency. The minimal latency of the adapter allows it to employ receive and transmit **FIFO** buffers which are small enough to be contained within RAM internal to an Application Specific Integrated Circuit (ASIC) containing the transceiver, ethernet controller, **FIFO** control circuitry and the host interface as well.

US PAT NO: 5,459,723 [IMAGE AVAILABLE] L6: 5 of 8
US-CL-CURRENT: **370/392**, **395**, **412**

ABSTRACT:
In a fast-packet **network**, incoming high-level data-link control (HDLC) data are supplied by a receiving line interface device to a packet management device comprising. . . packet management device has a transmitting state machine that rewrites the HDLC data from the frame buffer RAM to a **FIFO** register. When the **FIFO** register is **full** or entire data frame is in the **FIFO** register, the data are transferred to an HDLC transmitter coupled to a
transmitting line interface device.

US PAT NO: 5,412,782 [IMAGE AVAILABLE] L6: 6 of 8
US-CL-CURRENT: **395/250**; 364/239, 940.61, 940.62, DIG.1, DIG.2; **395/200.2**

ABSTRACT:
In a Local Area **Network** (LAN) system, an ethernet adapter exchanges data with a host through programmed I/O (PIO) and **FIFO** buffers. The receive PIO employs a DMA ring buffer backup so incoming packets can be copied directly into host memory when the PIO **FIFO** buffer is **full**. The adapter may be programmed to generate early receive interrupts when only a portion of a packet has been received from the **network**, so as to decrease latency. The adapter may also be programmed to generate a second early interrupt so that the. . . to the adapter, which further reduces latency. The minimal latency of the adapter allows it to employ receive and transmit **FIFO** buffers which are small enough to be contained within RAM internal to an Application Specific Integrated Circuit (ASIC) containing the transceiver, ethernet controller, **FIFO** control circuitry and the host interface as well.

US PAT NO: 5,406,554 [IMAGE AVAILABLE] L6: 7 of 8
US-CL-CURRENT: **370/381**; 365/189.01, 189.04, 189.08; **370/398**, **426**

ABSTRACT:
A synchronous first-in, first-out ("**FIFO**") having an alterable buffer store includes a dual-ported, random access memory ("RAM") based memory device incorporating conventional "**empty**" and "**full**" flags while also providing an alternate mode of operation in which the inhibiting effects of the "**empty**" and "**full**" flags are disabled whereby information contained within the **FIFO** may be modified before being read out. The alternate mode of operation is particularly useful in asynchronous transfer mode ("ATM")

networking applications.

US PAT NO: 4,814,980 [IMAGE AVAILABLE] L6: 8 of 8
US-CL-CURRENT: **395/200.03**; 364/228.3, 228.5, 229, 229.5, 231.9, 242.94, 244, 244.3, 260, 260.2, 263.2, 265, 266.3, 270.5, 270.7, 284, 284.3, 284.4, DIG.1; **395/200.2**

ABSTRACT:
A **network** of microprocessors, or nodes, are interconnected in an n-dimensional cube having bidirectional communication links along the edges of the n-dimensional cube. Each node's processor **network** includes an I/O subprocessor dedicated to controlling communication of message packets along a bidirectional communication link with each end thereof terminating at an I/O controlled transceiver. Transmit data lines are directly connected from a local **FIFO** through each node's communication link transceiver. Status and control signals from the neighboring nodes are delivered over supervisory lines to inform the local node that the neighbor node's **FIFO** is **empty** and the bidirectional link between the two nodes is idle for data communication. A clocking line between neighbors, clocks a message into an **empty** **FIFO** at a neighbor's node and vica versa. Either neighbor may acquire control over the bidirectional communication link at any time,. . . has circuitry for checking whether or not the communication link is busy or idle, and whether or not the receive **FIFO** is **empty**. Likewise, each node can **empty** its own **FIFO** and in turn deliver a status signal to a neighboring node indicating that the local **FIFO** is **empty**. The system includes features of automatic message rerouting, block message transfer and automatic parity checking and generation.

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